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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/047,809	01/15/2002	Ken Shoemaker	2207/12020	4746

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EXAMINER	
VO, LILIAN	
ART UNIT	**PAPER NUMBER**
2195	
MAIL DATE	**DELIVERY MODE**
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/047,809	SHOEMAKER ET AL.	
	Examiner	Art Unit	
	Lilian Vo	2195	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 February 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 - 28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 - 28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1 – 28 are pending.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1 - 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shiell et al. (US Pat. 5,913,049, hereinafter Shiell).

4. Regarding **claim 1**, Shiell discloses a multi-threading processor, comprising:

a first instruction fetch unit to receive a first thread and a second instruction fetch unit to receive a second thread (fig. 2: 260 and 261);

an execution unit to execute said first thread and said second thread (col. 9 lines 10 – 13, figs. 1 - 3); and

a multi-thread scheduler coupled to said first instruction fetch unit, said second instruction fetch unit, and said execution unit (fig. 2: 36), wherein said multi-thread scheduler is to determine the width of said execution unit (col. 8 line 56 – col. 9 line 13: "...scheduler 36 includes dependency check logic 58, which analyzes the mapped registers required by the Aops processed through register map logic 56 resource conflicts among themselves, and relative to

previously scheduled instructions...Once dependencies have been checked and handled...Schedule logic 60 compiles all information from these Aops and microcode instruction, and decides which instructions to launch to the execution units, in which order." Col. 14 lines 57 – 63 and col. 15 lines 15 - 25)

With respect to the limitation of multi-thread scheduler determines the width of the execution unit, Shiell discloses that "...scheduler 36 includes dependency check logic 58, which analyzes the mapped registers required by the Aops processed through register map logic 56 resource conflicts among themselves, and relative to previously scheduled instructions...Once dependencies have been checked and handled...Schedule logic 60 compiles all information from these Aops and microcode instruction, and decides which instructions to launch to the execution units, in which order" (col. 8 line 56 – col. 9 line 13) and the scheduling of the threads/instructions is based on the result of the communication corresponding thereto (col. 14 lines 57 – 63 and col. 15 lines 15 – 25). It is obvious that the width of the execution unit is been taking into consideration by the scheduler because each thread/instruction may require more or less bandwidth of the execution unit. Therefore, it would have been obvious for one of an ordinary skill in the art at the time the invention was made to recognize this limitation is taught by Shiell to fully utilize the available resource for the enhancement of system performance.

5. Regarding **claim 2**, Shiell discloses the multi-thread scheduler unit determines whether the execution unit is to execute the first thread and the second thread in parallel depending on the width of the execution unit (col. 8 line 56 – col. 9 line 13 and col. 14 line 57 – col. 15 line 15 – 25).

6. Regarding **claim 3**, Shiell discloses a multi-thread processor is an in-order processor (col. 1 line 29 – 35, col. 6 line 63 – col. 7 line 13, col. 8 line 56 – col. 9 line 13 and fig 3).

7. Regarding **claim 4**, Shiell discloses the execution unit executes the first thread and the second thread in parallel (col. 2 line 66 – col. 3 line 2).

8. Regarding **claim 5**, Shiell discloses the execution unit executes the first thread and the second thread in series (col. 6 line 63 – col. 7 line 13).

9. Regarding **claim 6**, Shiell discloses the first thread and the second thread are compiled to have instruction level parallelism (col. 1 lines 29 - 35).

10. Regarding **claim 7**, Shiell discloses a multi-threading processor comprising:

a first instruction decode unit coupled between the first instruction fetch unit and the multi-thread scheduler (fig. 2: 340); and

a second instruction decode unit coupled between the second instruction fetch unit and the multi-thread scheduler (fig 2: 341).

11. Regarding **claim 8,** Shiell discloses the execution unit executes only two threads in parallel (fig. 5: n+2 and n+3 cycles).

12. **Claims 9 – 28** are rejected on the same ground as stated in claims 1 – 8 above.

Response to Arguments

13. Applicant's arguments filed 2/15/07 have been fully considered but they are not persuasive for the reasons set forth below.

14. With respect to applicant's remark that "the Office Action dated November 15, 2006 admits that Shiell doe not disclose the element of applicants' claimed invention that states '...wherein said multi-thread scheduler is to determine the width of said execution unit'" (page 8 paragraph 3), the examiner disagrees. Nowhere in the Office Action states such admission.

In this case, Shiell discloses that "...scheduler 36 includes dependency check logic 58, which analyzes the mapped registers required by the Aops processed through register map logic 56 resource conflicts among themselves, and relative to previously scheduled instructions...Once dependencies have been checked and handled...Schedule logic 60 compiles all information from these Aops and microcode instruction, and decides which instructions to launch to the execution units, in which order" (col. 8 line 56 – col. 9 line 13) and the scheduling of the threads/instructions is based on the result of the communication corresponding thereto (col. 14 lines 57 – 63 and col. 15 lines 15 – 25). It is obvious that the width of the execution unit is been taking into consideration by the scheduler because each thread/instruction may require more or less bandwidth of the execution unit because Shiell clearly discloses that schedule logic 60 compiles all information from these Aops and microcode instructions and decides which instructions to launch to the execution units, in which order. Therefore, it would have been

obvious for one of an ordinary skill in the art at the time the invention was made to recognize this limitation is taught by Shiell to fully utilize the available resource for the enhancement of system performance.

If applicant believes these citations do not disclose such teaching or provide proper meaning of the claimed invention, applicant must provide a clear definition and the location of these limitations in the specification.

As noted by the Court of Customs and Patent Appeals, "argument cannot take the place of evidence." In re Langer, 503 F.2d 1380, 1395, 183 USPQ 288, 299 (CCPA 1974). In re Piasecki, 745 F.2d 1468, 1472, 223 USPQ 785 788 (Fed. Cir. 1984). Applicants have not submitted sufficient evidence to rebut the strong prima facie case of obviousness established by Examiner.

Furthermore, the examiner has interpreted the claim language as broadly as possible. It is also the examiner's position that applicant has not yet submitted claims drawn to limitations which define the method and system of applicant's disclosed invention in a manner that distinguishes over the prior art. Failure for applicant to significantly narrow definition/scope of the claims implies the applicant intends broad interpretation be given to the claims. The examiner thus maintains the rejections.

15. In response to applicant's argument that 'Shiell does not take the width of an execution unit consideration because each thread/instruction is sent to a different execution unit, there making determining the width unnecessary" (page 8 paragraph 4), the examiner disagrees. This passage merely states that when instructions are processed independently, it can be scheduled to

different execution units as Shiell discloses that one of the aspect of his invention is to provide a microprocessor and system in which multiple instructions may be processed independently and in parallel along much of the pipeline (col. 2 line 67 – col. 3 line 2).

Conclusion

16. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lilian Vo whose telephone number is 571-272-3774. The examiner can normally be reached on Thursday 8am - 5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng-Ai An can be reached on 571-272-3756. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Lilian Vo
Examiner
Art Unit 2195

lv
May 3, 2007

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